Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 9 are presently pending in the application. Claim 5 has been amended to more clearly set forth the claimed invention. Claim 9 has amended to correct a typographical error.

In paragraph 4 of the above-identified Office Action, claims 5 - 7 were rejected as being indefinite under 35 U.S.C. § 112, first paragraph. More specifically, it was alleged in the Office Action that the specification did not provide enablement for "currently reading out data being currently written in the memory from the microprocessor (See Claim 5, lines 15 - 17)", because, the claimed "microprocessor" did not have a memory for storing data. Claims 6 and 7 were rejected as depending from rejected claim 5. Claim 5 has been amended herein to make it even more clear that the data is being "read out ***by*** the microprocessor", rather than "***from*** the microprocessor" The limitation, as amended, is supported throughout the specification of the instant application. See, for example, the instant application on page 13, lines 22 - 23. It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, first paragraph.

In paragraph 6 of the Office Action, claims 1, 2 and 8 were rejected as allegedly being obvious under 35 U.S.C. § 103(a) over Applicant's Admitted Prior Art ("**AAPA**") in view of U. S. Patent No. 5,506,747 to Bain (called "Babin" in the Office Action, hereafter referred to as "**BAIN**") and U. S. Patent No. 5,841,722 to Willenz ("**WILLENZ**").

In paragraph 7 of the Office Action, claims 3, 4 and 9 were rejected as allegedly being obvious under 35 U.S.C. § 103(a) over **AAPA** in view of **BAIN** and **WILLENZ**, and further in view of U. S. Patent No.5,673,416 to Chee ("**CHEE**").

Applicant respectfully traverses the above rejections.

I. Applicant's claims require, among other limitations, a memory having a settable size, which size is set dynamically, in accordance with a size of contemporaneously transmitted data.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Applicant's claims require, among other limitations, **a memory having a settable size.** Applicant's claim 1 recites, among other limitations:

> "writing the digital data of a given HDLC-data frame from the first data bus to **a memory having a settable size**, said memory being arranged directly between said

first data bus and said second data bus;" [emphasis added by Applicant]

Applicant's independent claim 3 recites, among other limitations:

"writing the digital data from the first data bus to a **memory having a settable size**, said memory being arranged directly between said first data bus and said second data bus;" [emphasis added by Applicant]

Applicant's claim 5 recites, among other limitations:

"**a memory having a settable size** for storing data received from the first data bus and for subsequently reading out by the microprocessor,"

Further, the "**settable size**" of Applicant's claimed memory is determined dynamically, based on the size of the transmitted data to be written **contemporaneously** to the memory. For example, Applicant's claim 1 recites, among other limitations:

"**setting dynamically** via the microprocessor **a size** of the memory for **a current** reading/writing procedure of said memory;" [emphasis added by Applicant]

Applicant's independent claim 3 recites, among other limitations:

"setting dynamically via the microprocessor **a size** of the memory for a following reading/writing procedure of said memory, **the settable size being dependent on the size** of said transmitted HDLC-data frame **being written at the same time** in said memory;" [emphasis added by Applicant]

Applicant's independent claim 5 recites, among other limitations:

> "the **settable size** being **dependent on the size** of said transmitted HDLC-data frame **being written at the same time** in said memory;" [emphasis added by Applicant]

Both, 1) Applicant's **memory** having a **settable size; and** 2) the **size** being set, **dynamically** in accordance with a size of **contemporaneously** transmitted data, need to be found in the references in order to render Applicant's claims unpatentable. However, the references presently cited in the Office Action, neither teach, nor suggest, among other limitations of Applicant's claims, the two above-cited limitations.

II. The AAPA, BAIN, WILLENZ and CHEE references fail to teach or suggest, among other limitations of Applicant's claims, a memory having a settable size, which size is set dynamically, in accordance with a size of contemporaneously transmitted data.

As described in section I, above, both, 1) Applicant's **memory** having a **settable size; and** 2) the **size** being set, **dynamically** in accordance with a size of **contemporaneously** transmitted data, need to be found in the references in order to render Applicant's claims unpatentable. However, the references presently cited in the Office Action, neither teach, nor suggest, among other limitations of Applicant's claims, the two above-cited limitations.

More particularly, the **AAPA** cited in the specification of the instant application, **as noted in the Office Action on page 4, line 12**, fails to teach or suggest, among other limitations of Applicant's claims, **a settable memory**. More particularly, on page 4 of the Office Action, it was stated:

> "AAPA does not teach said memory being arranged directly between said first data bus and said second data bus, and **having a settable size**; and determining via said microprocessor from said memory control unit a quantity of said digital data to be read from said memory." [emphasis added by Applicant]

In failing to teach a **memory having a settable size**, the **AAPA** not only fails to teach Applicant's particularly claimed memory (point 1, above), but in so lacking such a teaching, cannot even be found to suggest Applicant's claimed invention where the size of the memory is dynamically set in accordance with contemporaneously sent data (point 2, above). As such, the **AAPA** reference fails to teach or suggest all of the limitations of Applicant's claimed invention, and Applicant's claims are patentable over the **AAPA** reference.

In addition to the above elements of Applicant's claims missing from the **AAPA**, the **AAPA** additionally fails to teach or suggest other elements of Applicant's claimed invention, such as the "informing" step of claim 1 and the **reading** of data, via the microprocessor. With regard to the **reading of data** of Applicant's claim 1, the **AAPA** only discloses a "**removal**" of

the data stored in the memory. However, the process of removal is neither identical to, nor equivalent to the process of reading. In fact, the process of removal is rather identical to the process of writing since the removal means that the respective memory portions are being written with a predefined logical value (i.e. "0") or an undefined state (i.e. "floating"). In the removal process of the **AAPA**, the data to be removed form the memory are never read out before. In summary, since the process of **removal** is not the same as the process of **reading**, as required by Applicant's claim 1, this feature is not disclosed in the **AAPA**. Nor does the **AAPA** perform Applicant's **informing** step of claim 1. The **AAPA** merely discloses that a microprocessor is informed if the received D-channel signals contain a byte indicating a frame end. This does not imply in the **AAPA** that the D-channel signals **are stored in the memory** in a way that the memory contains an entry indicating an end of a data frame.

Further, the **BAIN** reference cited in the Office Action, also fails to teach or suggest Applicant's particularly claimed **memory having a settable size**, and thus also cannot possibly teach or suggest that Applicant's particularly claimed **dynamic setting of the memory size in accordance with a size of contemporaneously sent data**. More particularly, the **BAIN** reference relates to provision of FIFO buffer in RAM. Rather

than resizing a memory, as required by Applicant's claims, **BAIN** teaches providing FIFOs having "various depths" in a RAM in a plurality of groups. See the **BAIN** Abstract. See also, Col. 2 of **BAIN**, lines 16 - 18, which states:

> "The addressing arrangement of the invention enables **many FIFOs of various sizes or depths to be provided in a RAM**, with very little storage requirement." [emphasis added by Applicant]

Having a plurality of FIFOs of different sizes in a RAM, is not the same as **dynamically sizing a memory in accordance with contemporaneously transmitted data**, as is required by Applicant's claims. The size of the FIFOs in **BAIN** are preset, and the RAM is pre-informed of the "depth" of each FIFO. See, **BAIN** col. 2, lines 25 - 41. In **BAIN**, the memory size is not set dynamically, as required by Applicant's claims. This is supported in the Office Action, on page 5, lines 1 - 2, which state:

> "AAPA, as modified by Babin [sic] does not teach setting dynamically via said microprocessor a size of said memory for a current reading/writing procedure of said memory."

The **BAIN** reference, like the **AAPA** fails to teach or suggest Applicant's limitations 1) and 2) above, among others. As such, the **BAIN** reference cannot be used to cure the deficiencies of the cited **AAPA** reference.

Nor does the **WILLENZ** reference cited in the Office Action, teach or suggest Applicant's particularly claimed **memory having a settable size**. On page 5 of the Office Action, lines 3 - 6, states:

> "Willenz discloses a variable sized FIFO buffer (See Fig. 1 and Abstract), wherein setting dynamically via a microprocessor (i.e., controller 16 of Figs. 1 and 2) a size of a memory (i.e., a variable size of FIFO buffer, viz., upper FIFO 10, lower FIFO, 12 and Random Access Memory 14 in Fig. 1, for a current reading/writing procedure of said memory (See col. 1, lines 26 - 29)."

Applicant respectfully disagrees with the above statement of what is allegedly taught by **WILLENZ**. Although **WILLENZ** states that it discloses a "variable sized" FIFO, it is not truly a "**memory having a settable size**" as claimed by Applicant. Rather, the **WILLENZ** reference discloses a FIFO including an upper FIFO buffer **of a fixed size**, a lower FIFO buffer **of a fixed size**, and a RAM. The RAM is utilized only when data can no longer flow between the upper and lower FIFO buffers, **due to the lower FIFO buffer being temporarily full**. See, the Abstract; col. 1, lines 36 - 50. The problem resulting from the arrangement taught **in the WILLENZ** reference is avoided by Applicant's claimed invention. In **WILLENZ** the upper and lower FIFO buffer may be temporarily full, since they are of fixed size. **In WILLENZ**, when one of the FIFO buffers is temporarily full, the data is latched into the RAM. Thus, the RAM is working as an additional buffer unit. However, neither the

upper FIFO buffer, nor the lower FIFO buffer, nor the RAM of **WILLENZ** have a **settable size**, as required by Applicant's claims. As such, the **WILLENZ** reference fails to teach a memory "**having a settable size**", as required by Applicant's claims.

Further, **WILLENZ** fails to teach or suggest that its so-called "variable-size" FIFO arrangement (the fixed size upper and lower FIFOs and RAM) has a size that is being **dynamically** set **contemporaneously** in accordance with the size of the data. Rather, col. 1 of **WILLENZ**, lines 26 - 28, states:

> "There is therefore provided, in accordance with a preferred embodiment of the present invention, a variable sized FIFO buffer whose size changes in accordance with how much data is present to be passed between the two systems."

The above is accomplished in **WILLENZ**, as stated in col. 3, lines 16 - 34, which states:

> "When the lower FIFO 12 reaches a full state (i.e. the indication from the lower flag unit 32 changes from a non-full indication to a full indication), control unit 44 indicates to the block combiner 46 to begin collecting the data flowing from the upper FIFO 10 into blocks. Typically, a block is eight words although other sized blocks can also be utilized. The size of the block is a function of the speed of the RAM 14. If, after the block has been created, the lower flag unit 32 still indicates fullness, the control unit 44 will initiate the writing of the block from block combiner 46 into RAM 14. This involves incrementing the write counter 38 to indicate the new address at which to write into the RAM 14, indicating to address MUX 42 to provide the output of the write counter 38 to the RAM

14 and providing a write (WR) signal to the RAM 14 (so that the RAM will perform the write operation).

Since RAM 14 acts as a first-in, first-out buffer, albeit with a single shared port, the blocks of words are sequentially written to it and are sequentially read out from it."

WILLENZ fails to teach or suggest a memory having a **settable size**, and **dynamically** changing the size of a **settable memory during** the data communication (see claim 1 "for a current reading/writing procedure"; and claims 3 and 5 "written at the same time"), as claimed by Applicant.

Additionally, the **CHEE** reference was cited in the Office Action on page 7, last paragraph, as allegedly disclosing a memory request and control unit. Even if, arguendo, **CHEE** were to teach the things alleged in the Office Action, **CHEE** neither teaches, nor suggests, a memory having **a settable size**, the size of which is set **dynamically** in accordance with **contemporaneously** transmitted data. As such, the **CHEE** reference cannot supply the missing elements that are neither taught, nor suggested, in the **AAPA**, **BAIN** and **WILLENZ** references.

III. Conclusion.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest

the features of claims 1, 3 or 5. Claims 1, 3 and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1, 3 or 5.

In view of the foregoing, reconsideration and allowance of claims 1 - 9 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Additionally, please consider the present as a petition for a one (1) month extension of time, and please provide a one month extension of time, to and including, January 29, 2005, to respond to the present Office Action.

The extension fee for response within a period of one (1) month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

Please provide any additional extensions of time that may be necessary and charge any other fees that might be due with

respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Applic. No. 09/398,689
Response Dated January 31, 2005
Responsive to Office Action of September 29, 2004

Respectfully submitted,

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For Applicant

KPS:cgm

January 31, 2005

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